RTL Specification Sheet

RAPID CPU Core Design

List of Pipeline Stages

1. IF --- Instruction Fetch
2. ID --- Instruction Decode
3. EX – Execute / ALU Stage
4. MEM – Memory Stage (Read & Write)
5. WB – Write backstage

TODO: make the TOC better

# 1.0 IF Stage

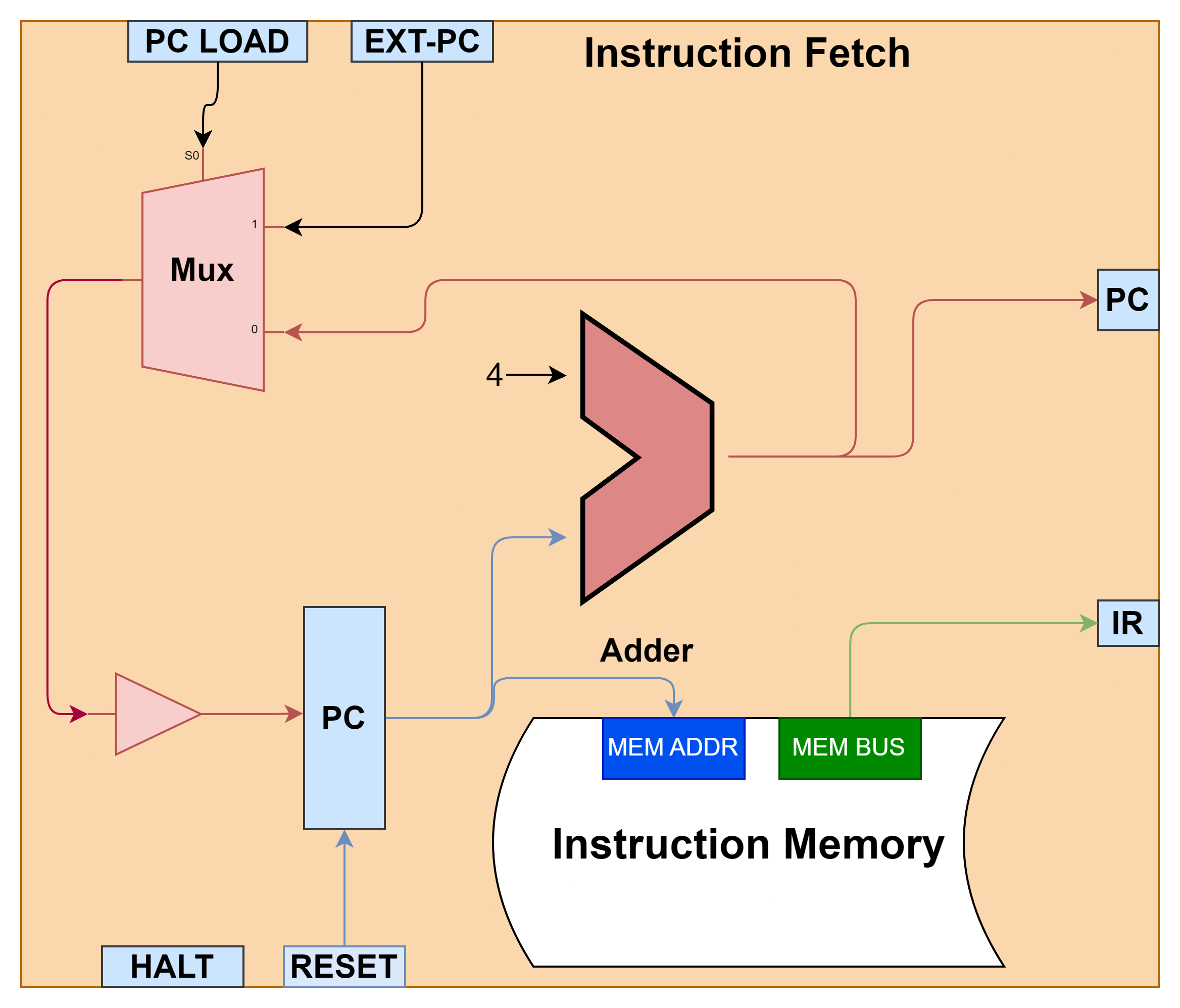
### 1.1 Purpose

To manage the program counter and interface with instruction cache block.

### 1.2 Requirements

1. Handle RESET signal.
2. Communicate with I-Cache interface
3. Allow for loading PC from external sources.
4. Handle synchronization by:
   1. Waiting until I-Cache is ready
   2. Waiting for pipeline ready flag before modifying PC
5. Ability to halt execution through an external signal.
6. Output ports are only modified when pipeline moves forward.

### 1.3 Block Diagram



### 1.4 State Machine

There are 5 states in the instruction fetch stage, the table below summarizes the objective of each state.

**State Description Table**

|  |  |  |
| --- | --- | --- |
| State # | State | Description |
| 1 | Fetch Instruction | Updates the memory address based on PC value IF stage waits in this state until memory read is complete. |
| 2 | Wait for Pipeline | IF moves to this state only from state #1 if pipeline ready flag is 0 and remains in this state until flag changes to 1. |
| 3 | Update output ports | Copies internal PC/instruction value to output ports and moves to state #4. Sets done flag to true. |
| 4 | Choose next PC value | Chooses between PC <- PC+4 OR PC <- EXT\_PC based on PC\_LOAD flag and then moves to state #4. Set done flag to false. |
| 5 | Halt | This state is entered only by EXT\_HALT flag and the IF stage does not exit this stage unless RESET flag is high. |

**State Transition Table**

|  |  |  |
| --- | --- | --- |
| Current State | Next State | Condition |
| 1 (FETCH) | 1 (FETCH) | REST=0, HALT=0, MEM\_READY = 0 |
| 1 (FETCH) | 2 (WAIT FOR PIPELINE) | REST=0, HALT=0, MEM\_READY =1, PIPELINE\_READY=0 |
| 1 (FETCH) | 3 (UPDATE PORTS) | REST=0, HALT=0, MEM\_READY =1, PIPELINE\_READY =1 |
| 2 (WAIT) | 2 (WAIT) | REST=0, HALT=0, PIPELINE\_READY =0 |
| 2 (WAIT) | 3 (UPDATE PORTS) | REST=0, HALT=0, PIPELINE\_READY =1 |
| 3 (UPDATE PORTS) | 4 (NEXT PC) | REST=0, HALT=0 |
| 4 (NEXT PC) | 1 (FETCH) | REST=0, HALT=0 |
| 5 (HALT) | 5 (HALT) | REST=0 |

### 1.5 State Diagram

### 1.6 Design Module I/O Ports

|  |  |  |
| --- | --- | --- |
| Type | Port | Summary |
| input | i\_clk | Clock signal |
| input | i\_reset | Reset signal |
| input | i\_pipeline\_ready | Synchronization signal w/ other pipeline stages. |
| input | i\_ext\_pc\_load | External flag to load i\_ext\_pc into pc. |
| input | i\_ext\_pc | External pc value used to branch pc. |
| output | o\_pc | Output PC value (set when i\_pipeline\_ready = 1) |
| output | o\_instruction | Output Instruction |
| output | o\_done | Output flag to signal done. |

# 2.0 ID Stage

### 2.1 Purpose

Decode

### 2.2 Requirements

# EX Stage

# MEM Stage

# WB Stage